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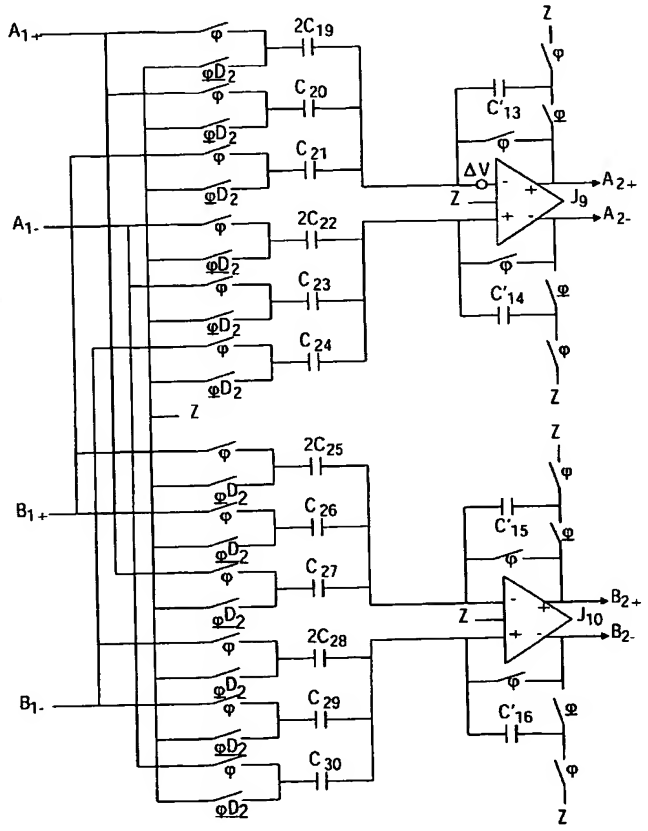
(54) Title: A DUAL RESIDUE PIPELINED AD CONVERTER



(57) Abstract: A dual residue pipelined AD converter comprising a cascade of, preferably balanced, switched capacitor dual residue converter stages for producing from first and second residue input signals one or more digital bits and first and second residue output signals for application to the nest stage in the cascade. Preferably the first and second residue input signals charge input capacitors whose charge is subsequently transferred to output capacitors by means of operational amplifiers. The switched capacitor architecture allows compensating for DC-offset voltages of the operational amplifiers. The switched capacitor architecture also allows the implementation of 1,5 bit converter stages.

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